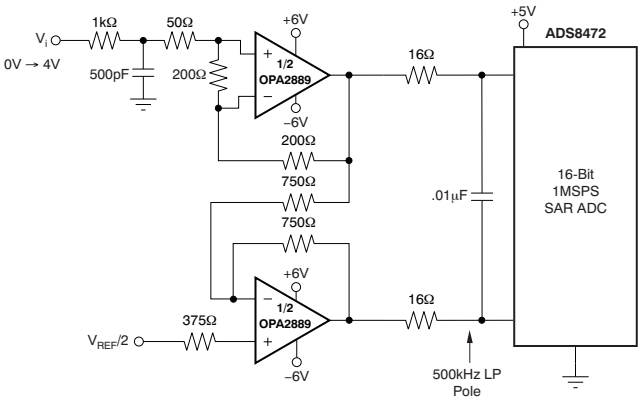
# Dual, Low-Power, Wideband, Voltage-Feedback OPERATIONAL AMPLIFIER with Disable

## FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  **+2.6V to +12V Single Supply**
  **±1.3V to ±6V Dual Supplies**
- **UNITY-GAIN STABLE**
- **WIDEBAND ±5V OPERATION: 60MHz (G = +2V/V)**
- **OUTPUT VOLTAGE SWING: ±4V**
- **HIGH SLEW RATE: 250V/μs**
- **LOW QUIESCENT CURRENT: 460μA/ch**
- **LOW DISABLE CURRENT: 18μA/ch**

## APPLICATIONS

- **VIDEO LINE DRIVING**
- **xDSL LINE RECEIVERS**
- **HIGH-SPEED IMAGING CHANNELS**
- **ADC BUFFERS**
- **PORTABLE INSTRUMENTS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **ACTIVE FILTERS**




**Low Power, DC-Coupled, Single-to-Differential Driver for ≤100kHz Inputs**

## DESCRIPTION

The OPA2889 represents a major step forward in unity-gain stable, voltage-feedback op amps. A new internal architecture provides slew rate and full-power bandwidth previously found only in wideband, current-feedback op amps. These capabilities give exceptional full-power bandwidth. Using a dual ±5V supply, the OPA2889 can deliver a ±4V output swing with over 40mA drive current and 60MHz bandwidth. This combination of features makes the OPA2889 an ideal RGB line driver or single-supply analog-to-digital converter (ADC) input driver or low power twisted pair line receiver.

The low 460μA/ch supply current of the OPA2889 is precisely trimmed at +25°C. System power may be reduced further using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, operates the OPA2889 normally. If pulled LOW, the OPA2889 supply current drops to less than 20μA/ch while the output goes into a high-impedance state.

### RELATED OPERATIONAL AMPLIFIER PRODUCTS

| | SINGLES | DUALS | TRIPLES |
|---|---|---|---|
| Low-Power Voltage-Feedback with Disable | OPA890 | OPA2890 | |
| Voltage-Feedback Amplifier with Disable (1800V/μs) | OPA690 | OPA2690 | OPA3690 |
| Current-Feedback Amplifier with Disable (2100V/μs) | OPA691 | OPA2691 | OPA3691 |
| Fixed Gain | OPA692 | | OPA3692 |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2007–2008, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| OPA2889 | SO-8 | D | –40°C to +85°C | OP2889 | OPA2889ID | Rail, 75 |
| | | | | | OPA2889IDR | Tape and Reel, 2500 |
| OPA2889 | MSOP-10 | DGS | –40°C to +85°C | BZY | OPA2889IDGST | Tape and Reel, 250 |
| | | | | | OPA2889IDGSR | Tape and Reel, 2500 |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

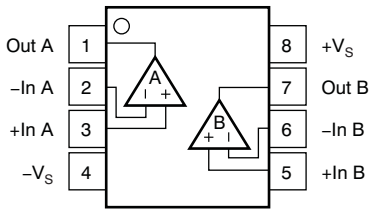
Over operating free-air temperature range, unless otherwise noted.

| | OPA2889 | UNIT |
|---|---|---|
| Power supply | ±6.5 | V |
| Internal power dissipation | See Thermal Characteristics | |
| Input voltage range | $\pm V_S$ | V |
| Storage temperature range | –65 to +125 | °C |
| Lead temperature (soldering, 10s) | +260 | °C |
| Maximum junction temperature ($T_J$) | +150 | °C |
| Maximum junction temperature ($T_J$), continuous operation | +140 | °C |
| ESD Rating: | | |
| Human body model (HBM) | 2000 | V |
| Charge device model (CDM) | 1000 | V |
| Machine model (MM) | 150 | V |

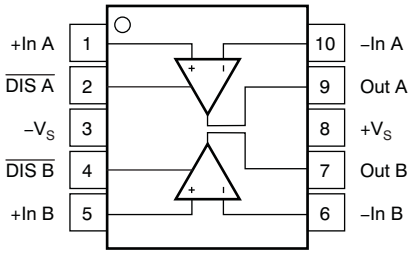
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## PIN ASSIGNMENTS

Top View SO-8




Top View MSOP-10





Copyright © 2007–2008, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±5V

At $T_A$ = +25°C, $R_F$ = 750Ω, G = +2V/V, and $R_L$ = 100Ω, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA2889ID, IDGS | | | | UNITS | MIN/MAX | TEST LEVEL (1) |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| | | +25°C | +25°C (2) | 0°C to +70°C (3) | –40°C to +85°C (3) | | | |
| **AC PERFORMANCE** | | | | | | | | |
| Small-Signal Bandwidth | G = +1V/V, $V_O$ = 100mV$_{PP}$, $R_F$ = 0Ω | 115 | | | | MHz | typ | C |
| | G = +2V/V, $V_O$ = 100mV$_{PP}$ | 60 | 40 | 36 | 32 | MHz | min | B |
| | G = +10V/V, $V_O$ = 100mV$_{PP}$ | 8 | 6 | 5 | 4.5 | MHz | min | B |
| Gain Bandwidth Product | G > +20V/V | 75 | 60 | 50 | 45 | MHz | min | B |
| Bandwidth for 0.1dB Flatness | G = +2V/V, $V_O$ = 100mV$_{PP}$ | 14 | | | | MHz | typ | C |
| Peaking at a Gain of +1V/V | $V_O$ < 100mV$_{PP}$ , $R_F$ = 0 Ω | 1 | | | | dB | typ | C |
| Large-Signal Bandwidth | G = +2V/V, $V_O$ = 2V$_{PP}$ | 70 | | | | MHz | typ | C |
| Slew Rate | G = +2V/V, $V_O$ = 2V Step | 250 | 175 | 160 | 150 | V/µs | min | B |
| Rise-and-Fall Time | 0.2V Step | 6 | | | | ns | typ | C |
| Settling Time to 0.02% | G = +1V/V, $V_O$ = 2V Step | 36 | | | | ns | typ | C |
| Settling Time to 0.1% | | 25 | | | | ns | typ | C |
| Harmonic Distortion | G = +2V/V, f = 1MHz, $V_O$ = 2V$_{PP}$ | | | | | | | |
| 2nd-Harmonic | $R_L$ = 200Ω | –75 | –65 | –62 | –60 | dBc | max | B |
| | $R_L$ ≥ 500Ω | –80 | –73 | –68 | –65 | dBc | max | B |
| 3rd-Harmonic | $R_L$ = 200Ω | –80 | –74 | –70 | –68 | dBc | max | B |
| | $R_L$ ≥ 500Ω | –82 | –80 | –75 | –72 | dBc | max | B |
| Input Voltage Noise | f > 100kHz | 8.4 | 10 | 11.5 | 12 | nV/√Hz | max | B |
| Input Current Noise | f > 100kHz | 0.7 | 1 | 1.2 | 1.4 | pA/√Hz | max | B |
| Differential Gain | G = +2V/V, $V_O$ = 1.4V$_{PP}$, $R_L$ = 150Ω | 0.06 | | | | % | typ | C |
| Differential Phase | G = +2V/V, $V_O$ = 1.4V$_{PP}$, $R_L$ = 150Ω | 0.04 | | | | ° | typ | C |
| Channel-to-Channel Crosstalk | f = 5MHz, Input-referred | –85 | | | | dB | typ | C |
| **DC PERFORMANCE (4)** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = 0V, $R_L$ = 100Ω | 66 | 60 | 58 | 57 | dB | min | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1.5 | ±5 | ±5.9 | ±6.3 | mV | max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | ±20 | ±20 | µV/°C | max | B |
| Input Bias Current | $V_{CM}$ = 0V | ±150 | ±750 | ±840 | ±880 | nA | max | A |
| Average Input Bias Current Drift | $V_{CM}$ = 0V | | | ±2 | ±2 | nA/°C | max | B |
| Input Offset Current | $V_{CM}$ = 0V | ±50 | ±200 | ±225 | ±235 | nA | max | A |
| Average Input Offset Current Drift | $V_{CM}$ = 0V | | | ±0.5 | ±0.5 | nA/°C | max | B |
| **INPUT** | | | | | | | | |
| Common-Mode Input Range (CMIR) (5) | | ±3.9 | ±3.8 | ±3.7 | ±3.6 | V | min | A |
| Common-Mode Rejection Ratio (CMRR) | $V_{CM}$ = 0V, Input-referred | 70 | 60 | 59 | 58 | dB | min | A |
| Input Impedance | | | | | | | | |
| Differential | $V_{CM}$ = 0V | 3.5 \|\| 0.5 | | | | MΩ \|\| pF | typ | C |
| Common-Mode | $V_{CM}$ = 0V | 170 \|\| 0.8 | | | | MΩ \|\| pF | typ | C |

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +4°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. $V_{CM}$ is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits

Copyright © 2007–2008, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $T_A$ = +25°C, $R_F$ = 750Ω, G = +2V/V, and $R_L$ = 100Ω, unless otherwise noted.

| | | OPA2889ID, IDGS | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C[2] | 0°C to +70°C[3] | –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
| **OUTPUT** | | | | | | | | |
| Output Voltage Swing | No load | ±4.0 | ±3.9 | ±3.8 | ±3.7 | V | min | A |
| | $R_L$ = 100Ω | ±3.3 | ±3.0 | ±2.95 | ±2.85 | V | min | A |
| Output Current, Sourcing, Sinking | $V_O$ = 0V | ±40 | ±28 | ±25 | ±22 | mA | min | A |
| Peak Output Current | Output shorted to ground | ±60 | | | | mA | typ | C |
| Closed-Loop Output Impedance | G = +2V/V, f = 100kHz | 0.04 | | | | Ω | typ | C |
| **DISABLE (MSOP-10 ONLY)** | Disable LOW | | | | | | | |
| Power-Down Supply Current (+$V_S$) | $V_{DIS}$ = 0, Both channels | 36 | 50 | 53 | 55 | µA | max | A |
| Disable Time | $V_{IN}$ = 1$V_{DC}$ | 70 | | | | µs | typ | C |
| Enable Time | $V_{IN}$ = 1$V_{DC}$ | 200 | | | | ns | typ | C |
| Off Isolation | G = +2V/V, f = 5MHz | 70 | | | | dB | typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | typ | C |
| Enable Voltage | | 3.3 | 3.4 | 3.5 | 3.55 | V | min | A |
| Disable Voltage | | 1.2 | 1.0 | 0.9 | 0.85 | V | max | A |
| Control Pin Input Bias Current ($V_{DIS}$) | $V_{DIS}$ = 0V, Each channel | 15 | 25 | 30 | 35 | µA | max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | ±5 | | | | V | typ | C |
| Minimum Operating Voltage | | | 1.3 | | | V | typ | C |
| Maximum Operating Voltage | | | ±6.0 | ±6.0 | ±6.0 | V | max | A |
| Maximum Quiescent Current | $V_S$ = ±5V, Both channels | 0.92 | 1 | 1.05 | 1.1 | mA | max | A |
| Minimum Quiescent Current | $V_S$ = ±5V, Both channels | 0.92 | 0.8 | 0.75 | 0.7 | mA | min | A |
| Power-Supply Rejection Ratio (+PSRR) | +$V_S$ = 4.5V to 5.5V | 64 | 62 | 61 | 60 | dB | min | A |
| (–PSRR) | –$V_S$ = –4.5V to –5.5V | 74 | 72 | 71 | 70 | dB | min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specified Operating Range D and DGS Packages | | –40 to +85 | | | | °C | typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-ambient | | | | | | | |
| D SO-8 | | 100 | | | | °C/W | typ | C |
| DGS MSOP-10 | | 135 | | | | °C/W | typ | |


Copyright © 2007–2008, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS: $V_S$ = +5V

At $T_A$ = +25°C, $R_F$ = 750Ω, G = +2V/V, and $R_L$ = 100Ω, unless otherwise noted.

| | | OPA2889ID, IDGS | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C(2) | 0°C to +70°C(3) | –40°C to +85°C(3) | UNITS | MIN/ MAX | TEST LEVEL(1) |
| **AC PERFORMANCE** | | | | | | | | |
| Small-Signal Bandwidth | G = +1V/V, $V_O$ = 100mV$_{PP}$, $R_F$ = 0Ω | 100 | | | | MHz | typ | C |
| | G = +2V/V, $V_O$ = 100mV$_{PP}$ | 50 | 30 | 26 | 22 | MHz | min | B |
| | G = +10V/V, $V_O$ = 100mV$_{PP}$ | 7 | 5.5 | 4.5 | 4 | MHz | min | B |
| Gain Bandwidth Product | G > +20V/V | 70 | 55 | 45 | 40 | MHz | min | B |
| Bandwidth for 0.1dB Flatness | G = +2V/V, $V_O$ = 100mV$_{PP}$ | 14 | | | | MHz | typ | C |
| Peaking at a Gain of +1V/V | $V_O$ < 100mV$_{PP}$ , $R_F$ = 0 Ω | 1 | | | | dB | typ | C |
| Large-Signal Bandwidth | G = +2V/V, $V_O$ = 2V$_{PP}$ | 60 | | | | MHz | typ | C |
| Slew Rate | G = +2V/V, $V_O$ = 2V Step | 200 | 125 | 110 | 100 | V/µs | min | B |
| Rise-and-Fall Time | 0.2V Step | 6.5 | | | | ns | typ | C |
| Settling Time to 0.02% | G = +1V/V, $V_O$ = 2V Step | 38 | | | | ns | typ | C |
| Settling Time to 0.1% | | 27 | | | | ns | typ | C |
| Harmonic Distortion | G = +2V/V, f = 1MHz, $V_O$ = 2V$_{PP}$ | | | | | | | |
| 2nd-Harmonic | $R_L$ = 200Ω | –71 | –61 | –58 | –56 | dBc | max | B |
| | $R_L$ ≥ 500Ω | –76 | –69 | –64 | –61 | dBc | max | B |
| 3rd-Harmonic | $R_L$ = 200Ω | –76 | –70 | –66 | –64 | dBc | max | B |
| | $R_L$ ≥ 500Ω | –76 | –74 | –69 | –66 | dBc | max | B |
| Input Voltage Noise | f > 100kHz | 8.5 | 10.5 | 12 | 12.5 | nV/√Hz | max | B |
| Input Current Noise | f > 100kHz | 0.7 | 1 | 1.1 | 1.2 | pA/√Hz | max | B |
| Differential Gain | G = +2V/V, $V_O$ = 1.4V$_{PP}$, $R_L$ = 150Ω | 0.06 | | | | % | typ | C |
| Differential Phase | G = +2V/V, $V_O$ = 1.4V$_{PP}$, $R_L$ = 150Ω | 0.04 | | | | ° | typ | C |
| Channel-to-Channel Crosstalk | f = 5MHz, Input-referred | –85 | | | | dB | typ | C |
| **DC PERFORMANCE(4)** | | | | | | | | |
| Open-Loop Voltage Gain ($A_{OL}$) | $V_O$ = 0V, $R_L$ = 100Ω | 64 | 58 | 56 | 55 | dB | min | A |
| Input Offset Voltage | $V_{CM}$ = 0V | ±1.5 | ±5 | ±5.9 | ±6.3 | mV | max | A |
| Average Offset Voltage Drift | $V_{CM}$ = 0V | | | ±20 | ±20 | µV/°C | max | B |
| Input Bias Current | $V_{CM}$ = 0V | ±150 | ±800 | ±890 | ±930 | nA | max | A |
| Average Input Bias Current Drift | $V_{CM}$ = 0V | | | ±2 | ±2 | nA/°C | max | B |
| Input Offset Current | $V_{CM}$ = 0V | ±50 | ±250 | ±275 | ±285 | nA | max | A |
| Average Input Offset Current Drift | $V_{CM}$ = 0V | | | ±0.5 | ±0.5 | nA/°C | max | B |
| **INPUT** | | | | | | | | |
| Most Positive Input Voltage | | 4 | 3.9 | 3.8 | 3.75 | V | min | A |
| Least Positive Input Voltage | | 1 | 1.1 | 1.2 | 1.25 | V | max | A |
| Common-Mode Rejection Ratio (CMRR) | $V_{CM}$ = 0V, Input-referred | 68 | 58 | 57 | 56 | dB | min | A |
| Input Impedance | | | | | | | | |
| Differential | $V_{CM}$ = 0V | 3.5 \|\| 0.5 | | | | MΩ \|\| pF | typ | C |
| Common-Mode | $V_{CM}$ = 0V | 170 \|\| 0.8 | | | | MΩ \|\| pF | typ | C |

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +4°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. $V_{CM}$ is the input common-mode voltage.

Copyright © 2007–2008, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS: $V_S$ = +5V (continued)

At $T_A$ = +25°C, $R_F$ = 750Ω, G = +2V/V, and $R_L$ = 100Ω, unless otherwise noted.

| | | OPA2889ID, IDGS | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C[2] | 0°C to +70°C[3] | –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
| **OUTPUT** | | | | | | | | |
| Most Positive Output Voltage | No load | 4 | 3.9 | 3.8 | 3.7 | V | min | A |
| | $R_L$ = 100Ω | 3.85 | 3.7 | 3.6 | 3.55 | V | min | A |
| Least Positive Output Voltage | No Load | 1 | 1.1 | 1.2 | 1.3 | V | max | A |
| | $R_L$ = 100Ω | 1.15 | 1.3 | 1.4 | 1.45 | V | max | A |
| Output Current, Sourcing, Sinking | $V_O$ = 0V | ±35 | ±24 | ±21 | ±18 | mA | min | A |
| Peak Output Current | Output shorted to ground | ±50 | | | | mA | typ | C |
| Closed-Loop Output Impedance | G = +2V/V, f = 100kHz | 0.04 | | | | Ω | typ | C |
| **DISABLE (MSOP-10 ONLY)** | Disable LOW | | | | | | | |
| Power-Down Supply Current (+$V_S$) | $V_{DIS}$ = 0, both channels | 36 | 50 | 53 | 55 | µA | max | A |
| Disable Time | $V_{IN}$ = 1$V_{DC}$ | 70 | | | | µs | typ | C |
| Enable Time | $V_{IN}$ = 1$V_{DC}$ | 200 | | | | ns | typ | C |
| Off Isolation | G = +2V/V, f = 5MHz | 70 | | | | dB | typ | C |
| Output Capacitance in Disable | | 4 | | | | pF | typ | C |
| Enable Voltage | | 3.3 | 3.4 | 3.5 | 3.55 | V | min | A |
| Disable Voltage | | 1.2 | 1.0 | 0.9 | 0.85 | V | max | A |
| Control Pin Input Bias Current ($V_{DIS}$) | $V_{DIS}$ = 0V, Each channel | 15 | 25 | 30 | 35 | µA | max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified Operating Voltage | | +5 | | | | V | typ | C |
| Minimum Operating Voltage | | | +2.6 | | | V | typ | C |
| Maximum Operating Voltage | | | +12 | +12 | +12 | V | max | A |
| Maximum Quiescent Current | $V_S$ = +5V, Both channels | 0.85 | 0.95 | 1.0 | 1.05 | mA | max | A |
| Minimum Quiescent Current | $V_S$ = +5V, Both channels | 0.85 | 0.75 | 0.7 | 0.65 | mA | min | A |
| Power-Supply Rejection (+PSRR) Ratio | +$V_S$ = 4.5V to 5.5V | 60 | | | | dB | typ | C |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specified Operating Range D and DGS Packages | | –40 to +85 | | | | °C | typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-ambient | | | | | | | |
| D SO-8 | | 100 | | | | °C/W | typ | C |
| DGS MSOP-10 | | 135 | | | | °C/W | typ | C |


Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 50.

**SMALL-SIGNAL FREQUENCY RESPONSE**

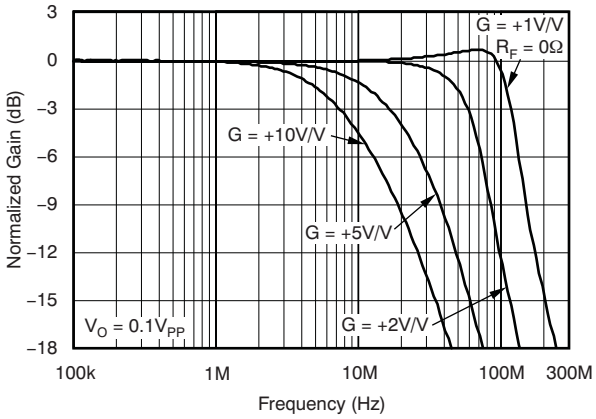



**Figure 1.**

**LARGE-SIGNAL FREQUENCY RESPONSE**

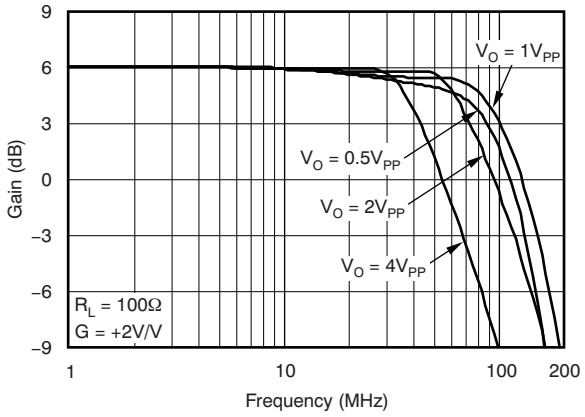



**Figure 2.**

**SMALL-SIGNAL PULSE RESPONSE**

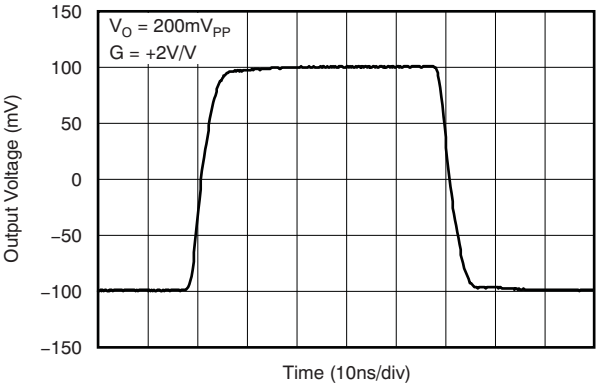



**Figure 3.**

**LARGE-SIGNAL PULSE RESPONSE**

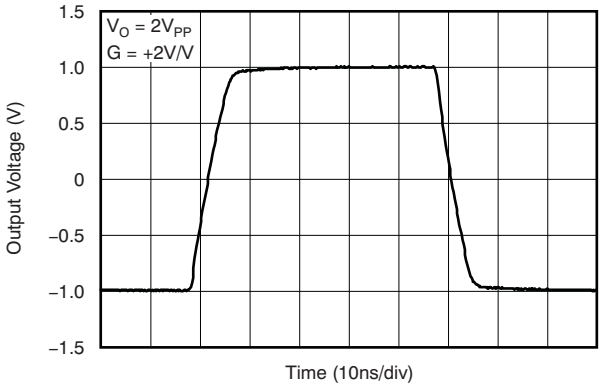



**Figure 4.**

**VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE**

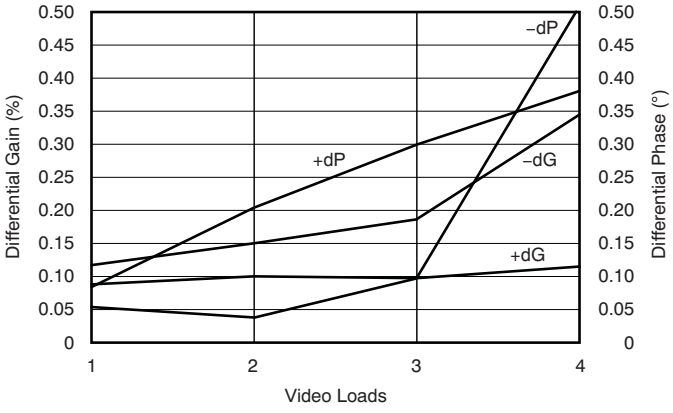



**Figure 5.**

**CHANNEL-TO-CHANNEL CROSSTALK**

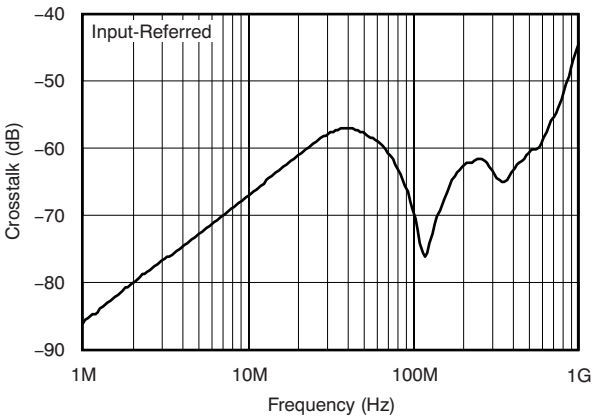



**Figure 6.**

Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 50.

HARMONIC DISTORTION vs LOAD RESISTANCE

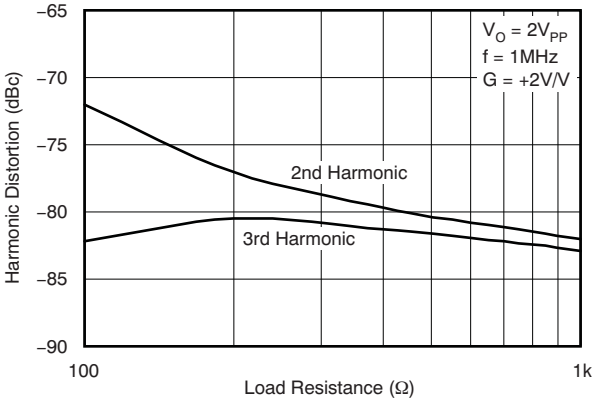



Figure 7.

1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

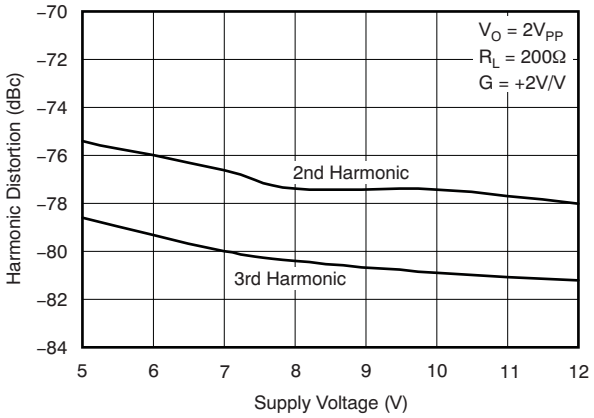



Figure 8.

HARMONIC DISTORTION vs FREQUENCY

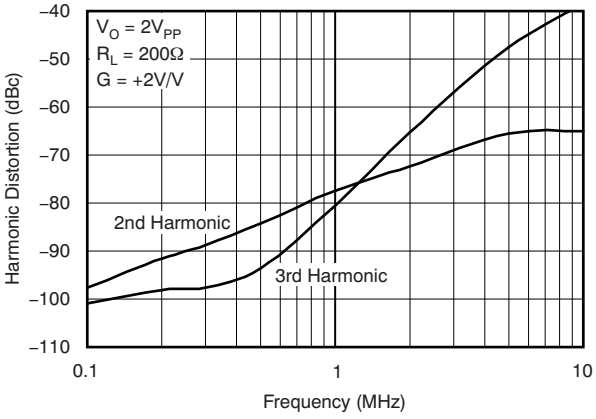



Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

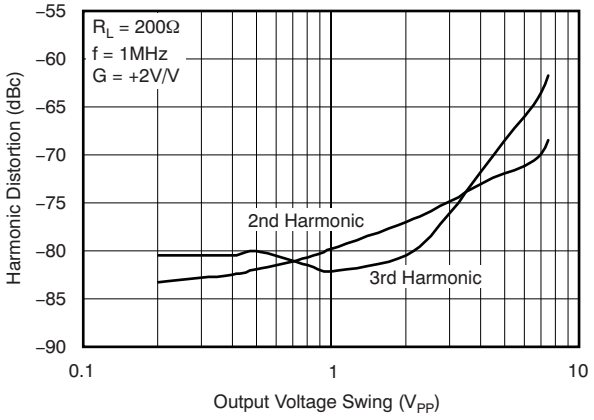



Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

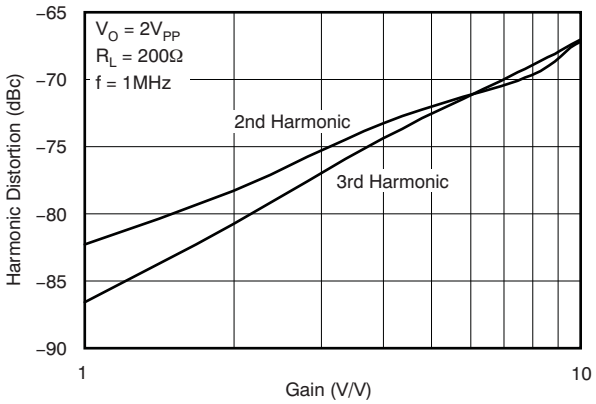



Figure 11.

HARMONIC DISTORTION vs INVERTING GAIN

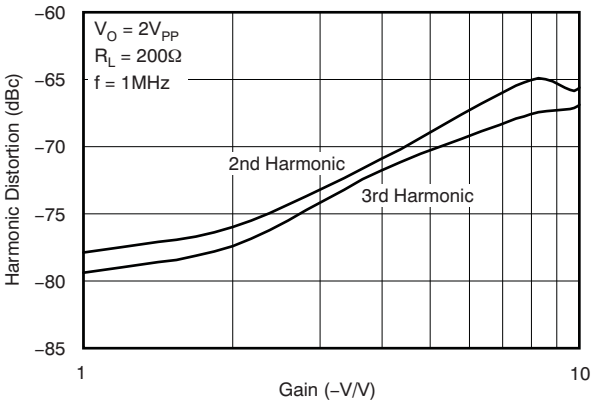



Figure 12.


Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 50.

**LOW-FREQUENCY INVERTING HARMONIC DISTORTION**

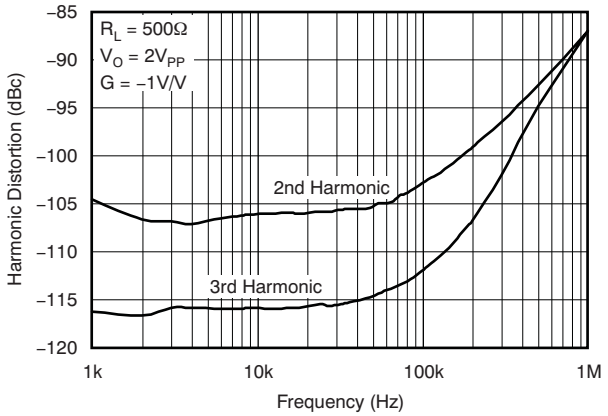



**Figure 13.**

**TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS**

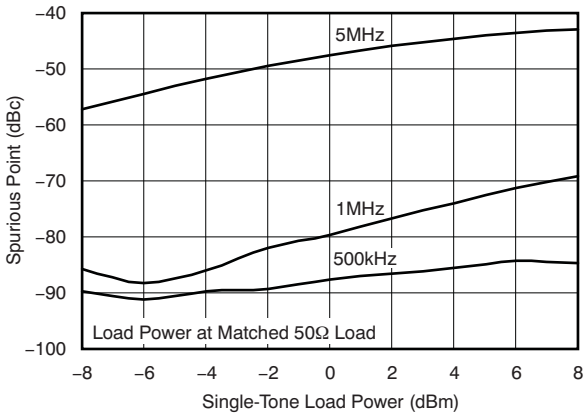



**Figure 14.**

**RECOMMENDED $R_S$ vs CAPACITIVE LOAD**

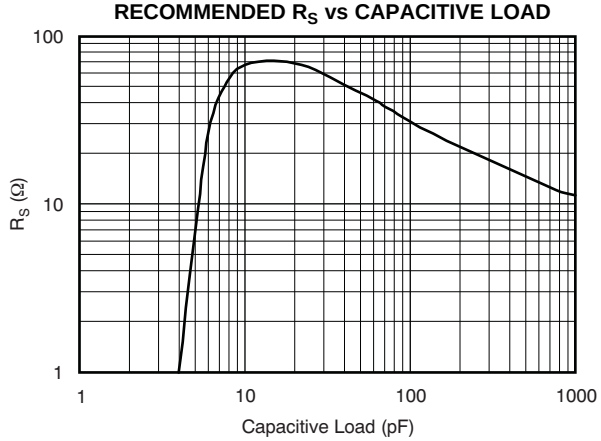



**Figure 15.**

**FREQUENCY RESPONSE vs CAPACITIVE LOAD**

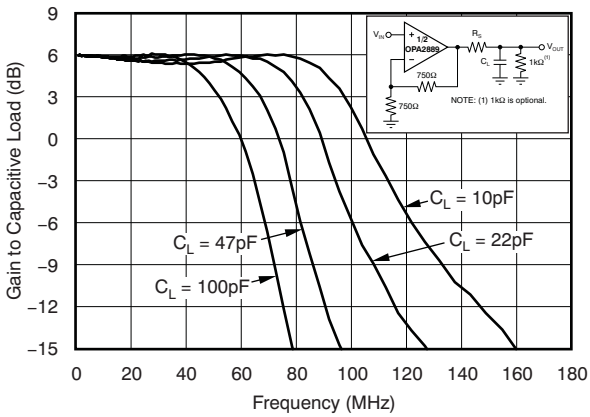



**Figure 16.**

**COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

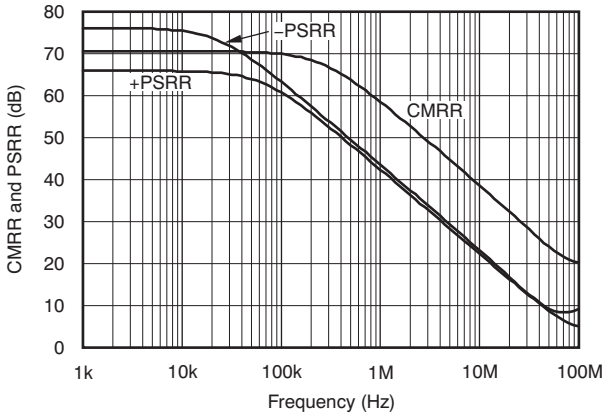



**Figure 17.**

**INPUT VOLTAGE AND CURRENT NOISE**

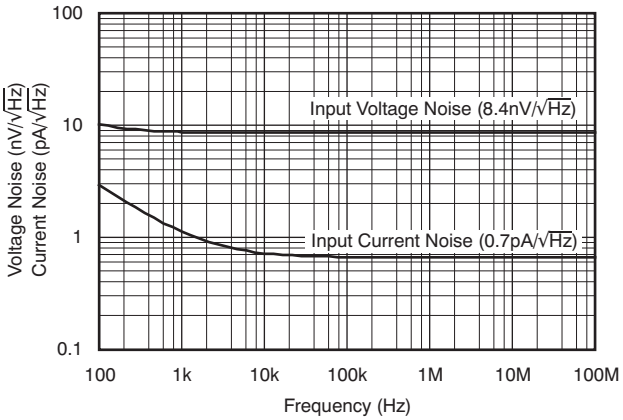



**Figure 18.**

Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 50.

**SUPPLY AND OUTPUT CURRENT vs TEMPERATURE**

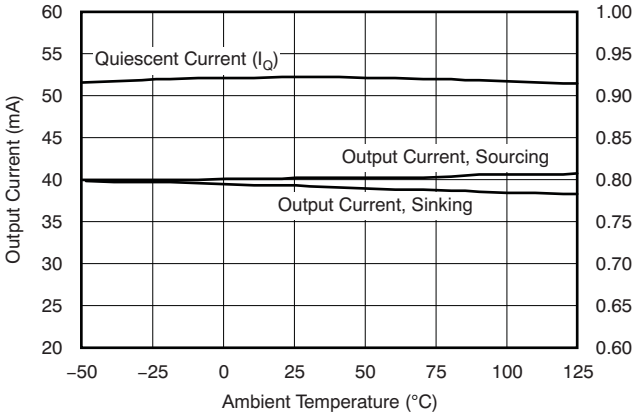



**Figure 19.**

**TYPICAL DC DRIFT OVER TEMPERATURE**

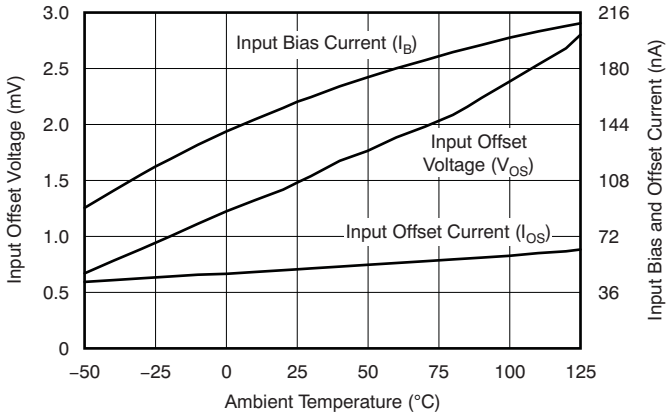



**Figure 20.**

**LARGE-SIGNAL DISABLE/ENABLE RESPONSE**

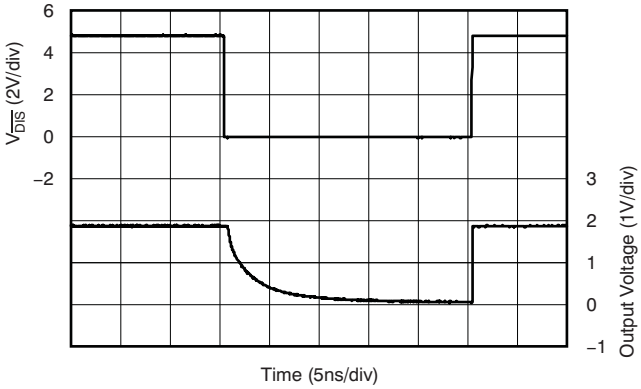



**Figure 21.**

**NONINVERTING OVERDRIVE RECOVERY**

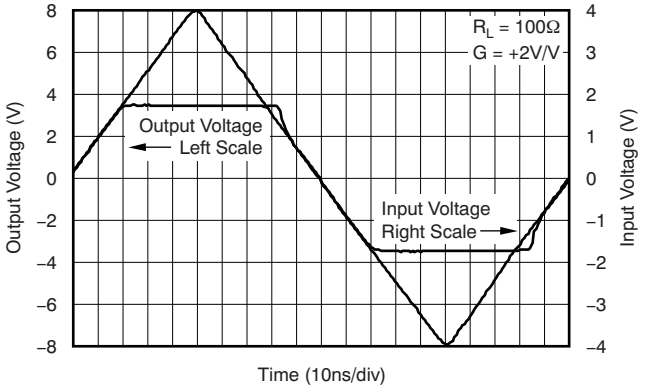



**Figure 22.**

**CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

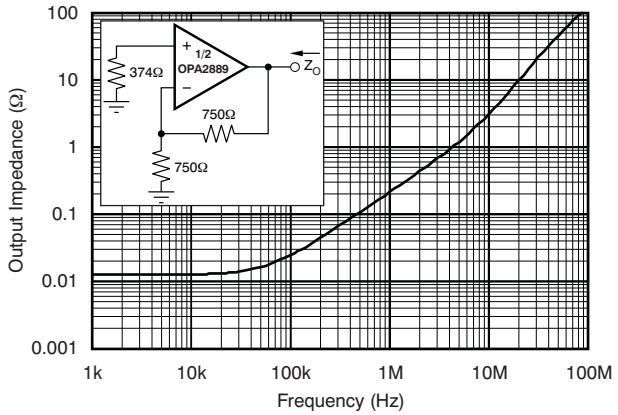



**Figure 23.**

**OPEN-LOOP GAIN AND PHASE**

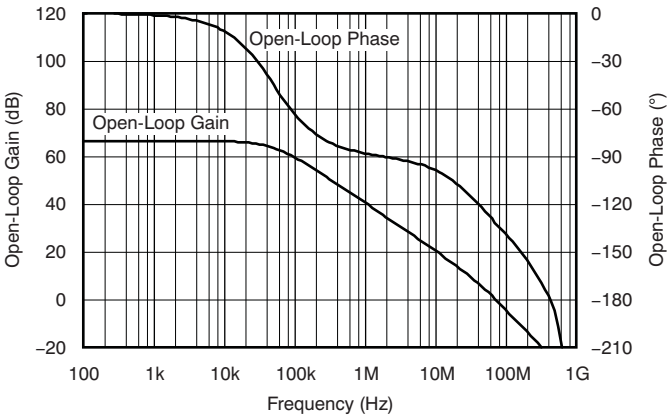



**Figure 24.**


Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 50.

**DISABLE FEEDTHROUGH**

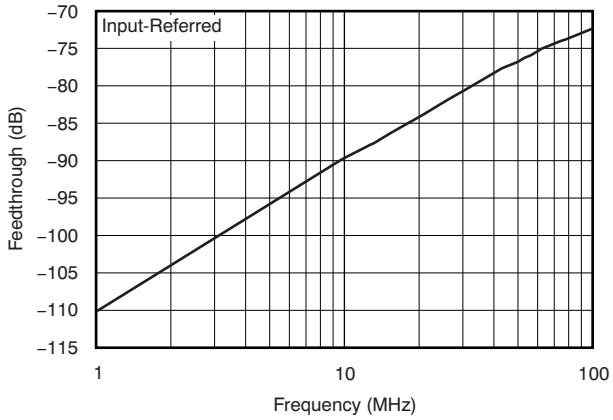



**Figure 25.**

**COMMON-MODE AND DIFFERENTIAL INPUT IMPEDANCE**

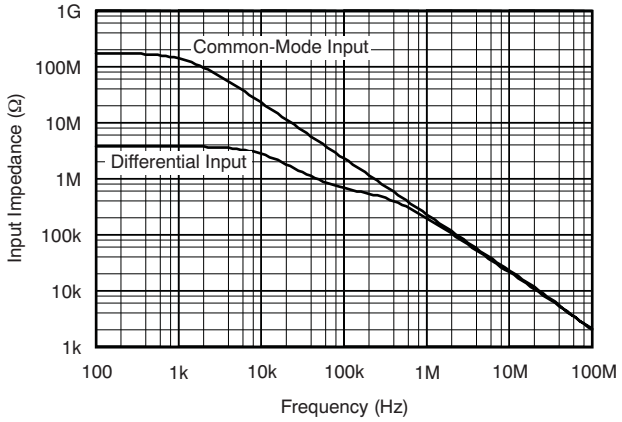



**Figure 26.**

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V, Differential

At $T_A$ = +25°C, Differential Gain = +2V/V, and $R_L$ = 200Ω, unless otherwise noted. See Figure 52 and Figure 53.

**DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE**

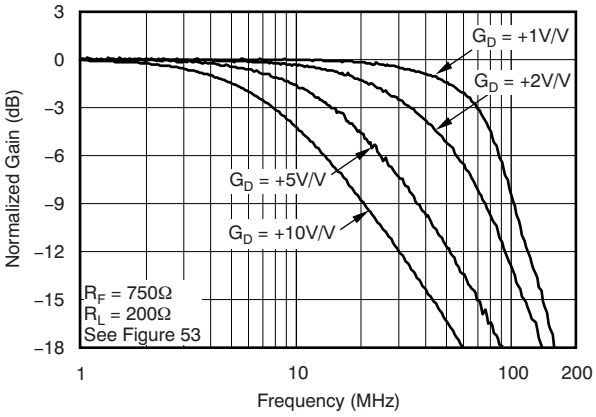



**Figure 27.**

**DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE**

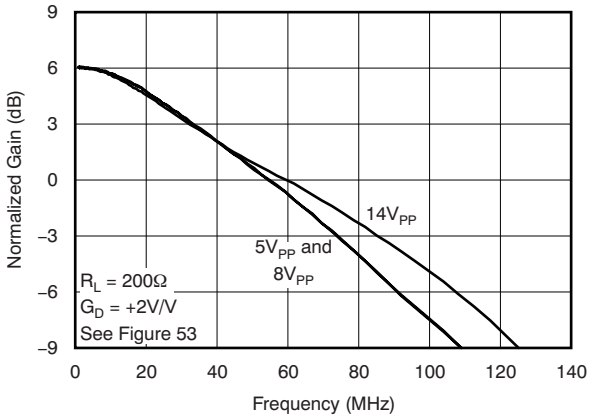



**Figure 28.**

**DIFFERENTIAL DISTORTION vs LOAD RESISTANCE**

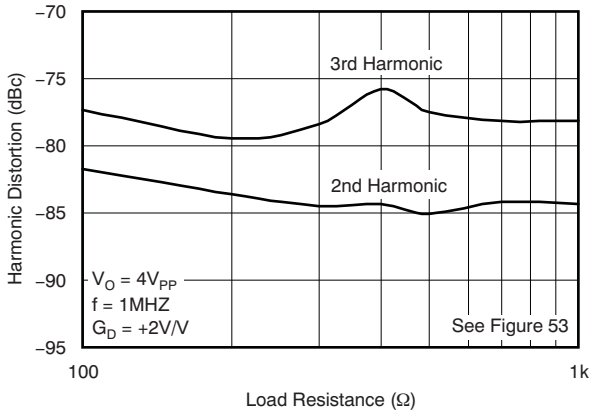



**Figure 29.**

**DIFFERENTIAL DISTORTION vs FREQUENCY**

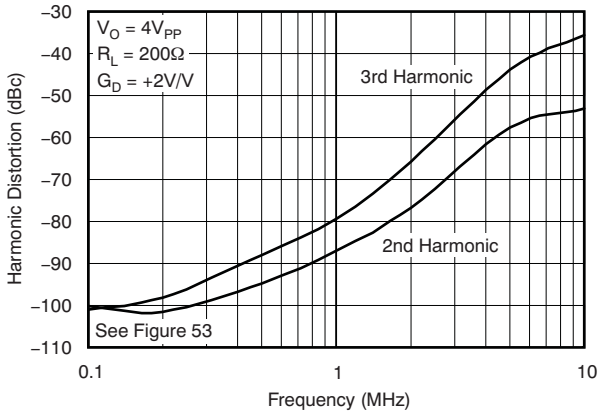



**Figure 30.**

**DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE**

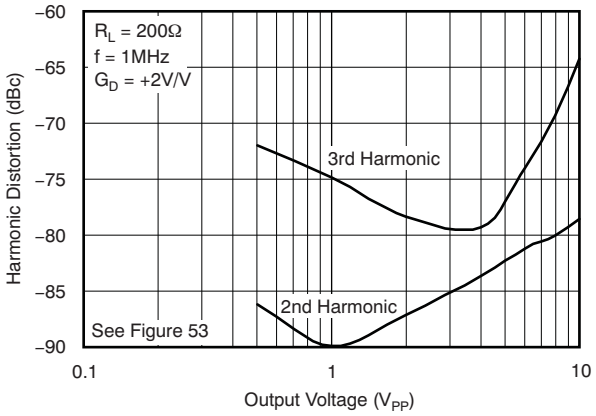



**Figure 31.**

**DIFFERENTIAL DISTORTION vs FREQUENCY**

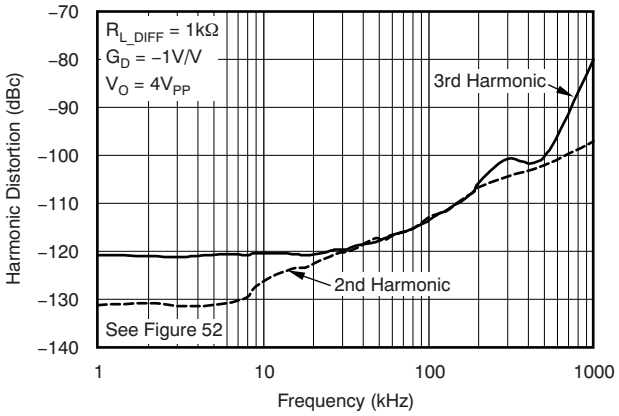



**Figure 32.**


Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = +5V

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 51.

**NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE**

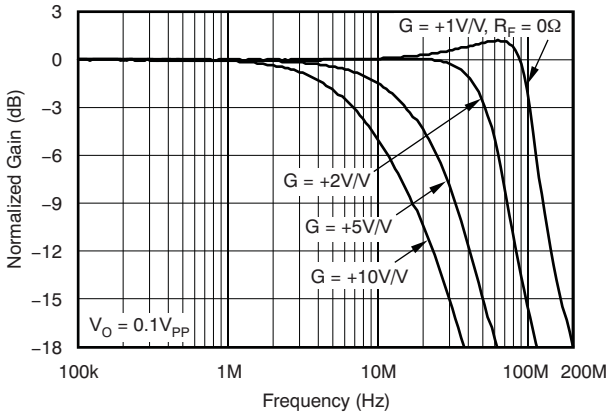



**Figure 33.**

**NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE**

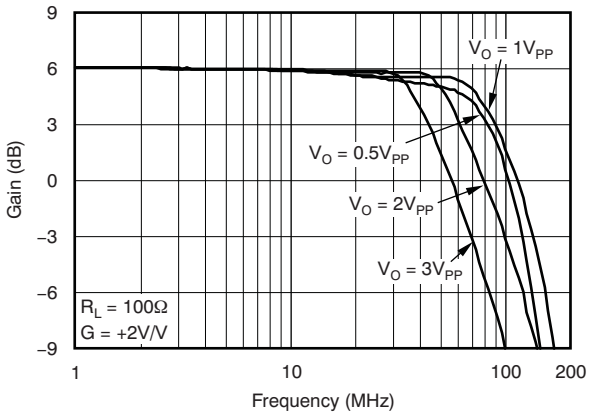



**Figure 34.**

**SMALL-SIGNAL PULSE RESPONSE**

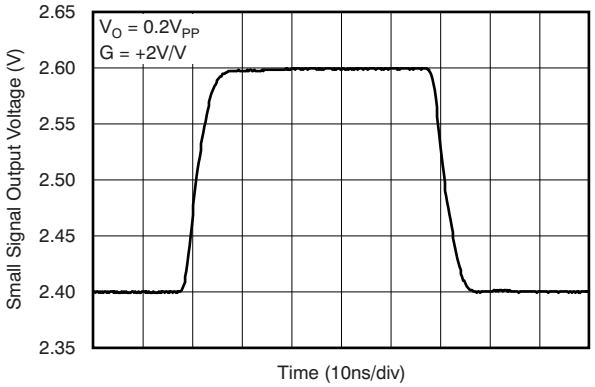



**Figure 35.**

**LARGE-SIGNAL PULSE RESPONSE**

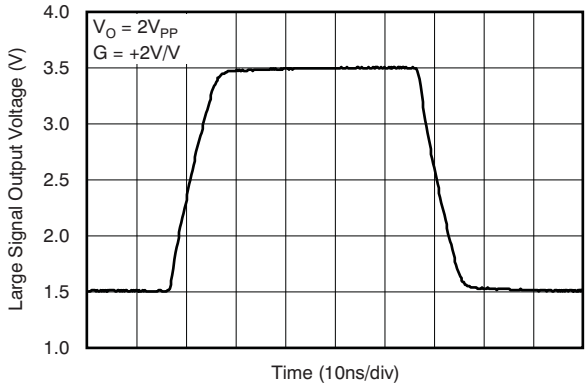



**Figure 36.**

**RECOMMENDED $R_S$ vs CAPACITIVE LOAD**

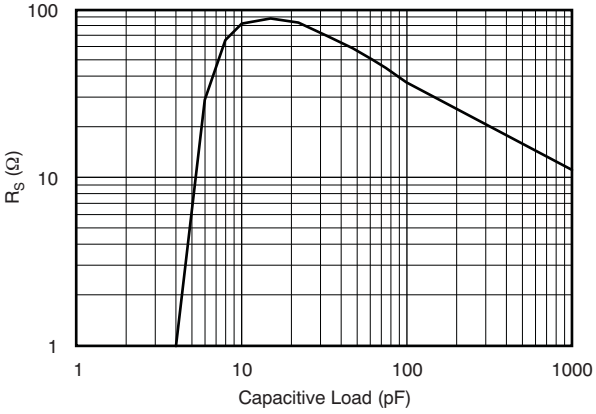



**Figure 37.**

**FREQUENCY RESPONSE vs CAPACITIVE LOAD**

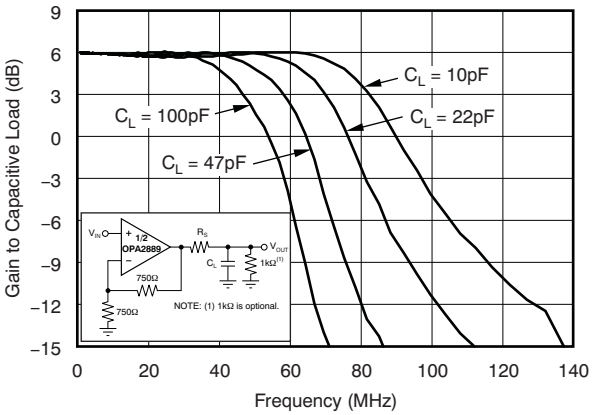



**Figure 38.**

Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = +5V (continued)

At $T_A$ = +25°C, G = +2V/V, $R_F$ = 750Ω, and $R_L$ = 100Ω, unless otherwise noted. See Figure 51.

**NONINVERTING OVERDRIVE RECOVERY**

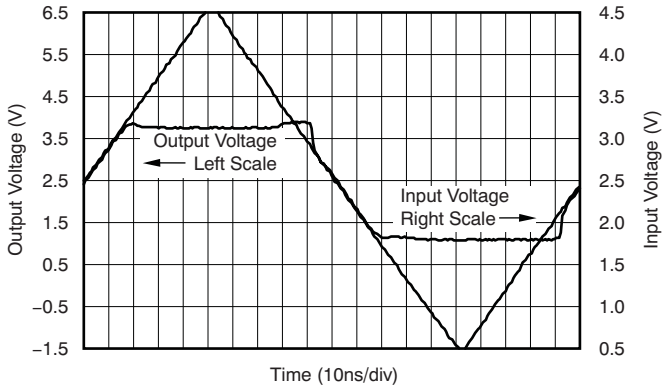



**Figure 39.**

**HARMONIC DISTORTION vs LOAD RESISTANCE**

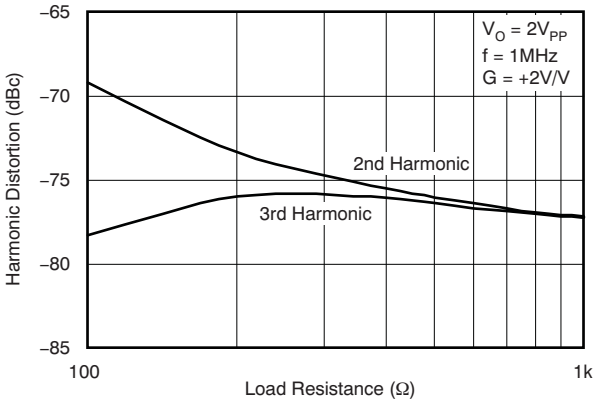



**Figure 40.**

**HARMONIC DISTORTION vs FREQUENCY**

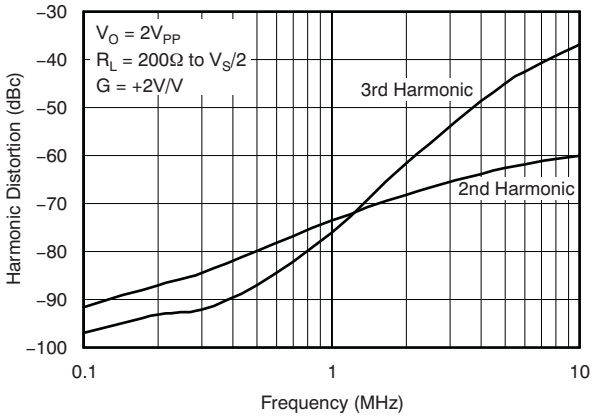



**Figure 41.**

**HARMONIC DISTORTION vs OUTPUT VOLTAGE**

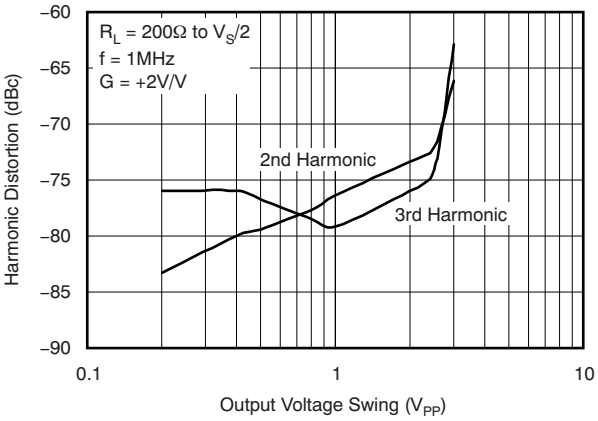



**Figure 42.**

**HARMONIC DISTORTION vs NONINVERTING GAIN**

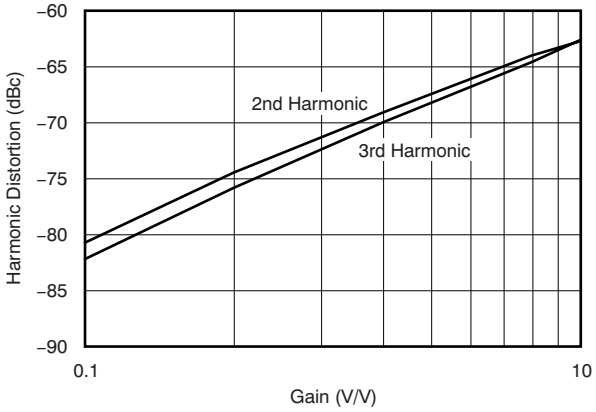



**Figure 43.**

**TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS**

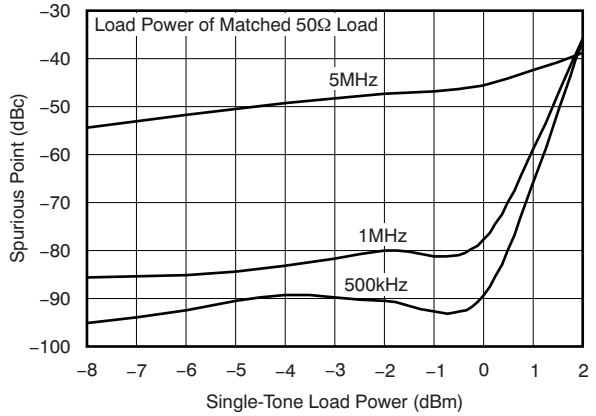



**Figure 44.**


Copyright © 2007–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS: $V_S$ = +5V, Differential

At $T_A$ = +25°C, Differential Gain = +2V/V, and $R_L$ = 200Ω, unless otherwise noted. See Figure 52.

**DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE**

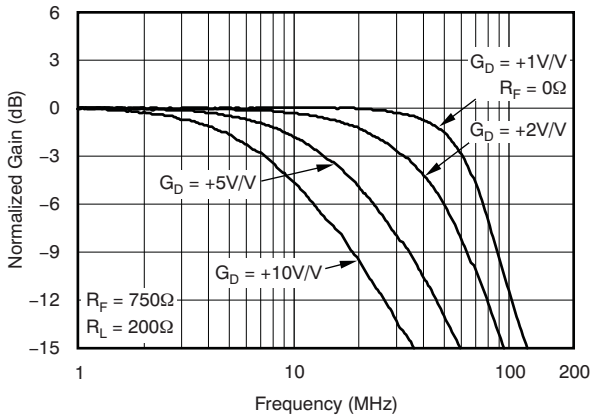



**Figure 45.**

**DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE**

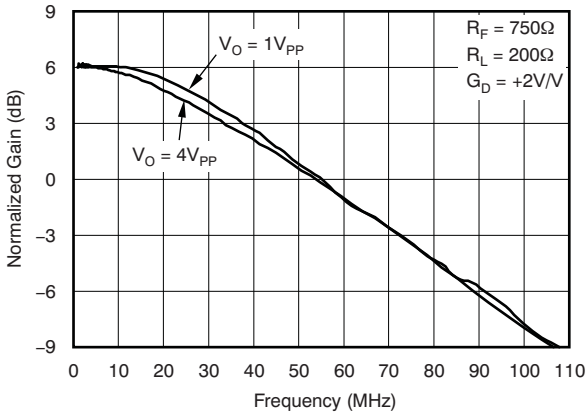



**Figure 46.**

**DIFFERENTIAL DISTORTION vs LOAD RESISTANCE**

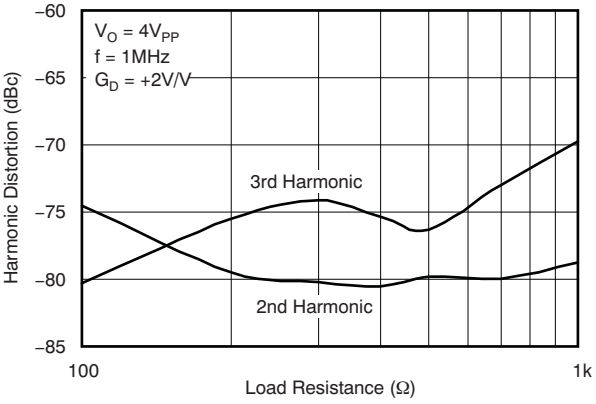



**Figure 47.**

**DIFFERENTIAL DISTORTION vs FREQUENCY**

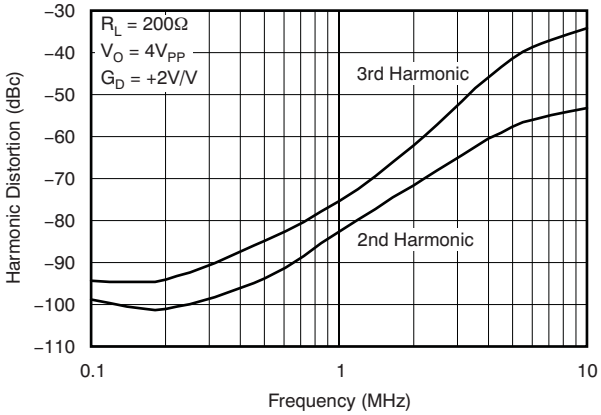



**Figure 48.**

**DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE**

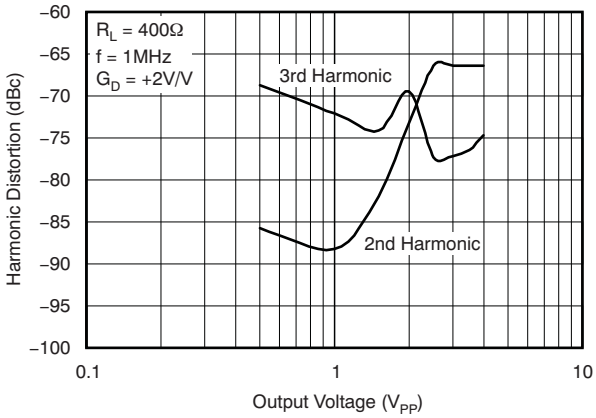



**Figure 49.**

Copyright © 2007–2008, Texas Instruments Incorporated

## APPLICATIONS INFORMATION

### WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA2889 provides an exceptional combination of high output power capability in a dual, wideband, unity-gain stable, voltage-feedback op amp using a new high slew rate input stage. Typical differential input stages used for voltage-feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA2889 uses a new input stage that places the transconductance element between two input buffers, using the output currents as the forward signal. As the error voltage increases across the two inputs, an increasing current is delivered to the compensation capacitor. This configuration provides high slew rate (250V/µs) while consuming very low quiescent current (460µA/ch). This exceptional full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures. The 8.4nV/√Hz input voltage noise for the OPA2889 is exceptionally low for this type of input stage.

Figure 50 shows the dc-coupled, gain of +2V/V, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and ±5V Typical Chararacteristics. This illustration is for one channel; the other channel is connected similarly. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 100Ω. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 50, the total effective load will be 100Ω || 1.5kΩ. The disable control line (MSOP-10 package only) is typically left open for normal amplifier operation. Two optional components are included in Figure 50. An additional resistor (350Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this resistor gives an input bias current cancelling resistance that matches the 375Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional-added capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

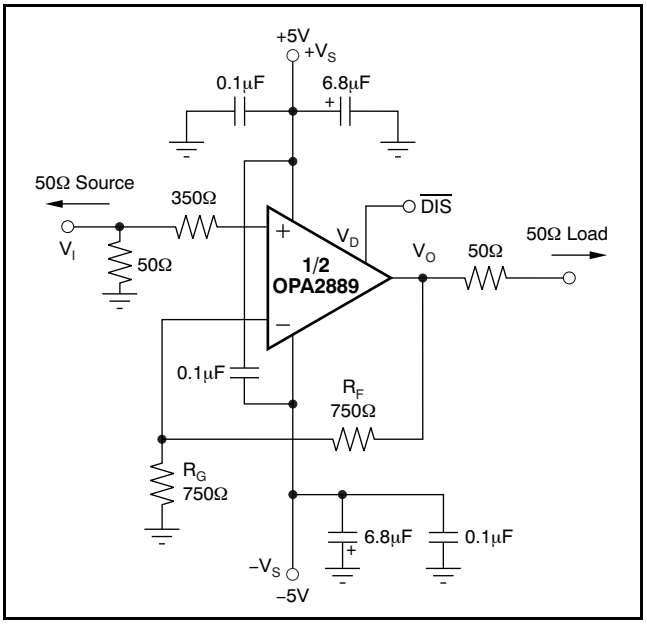



**Figure 50. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit**

Figure 51 illustrates the ac-coupled, gain of +2V/V, single-supply circuit configuration used as the basis of the +5V Electrical Characteristics and +5V Typical Chararacteristics. Though not a rail-to-rail design, the OPA2889 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. It delivers a $2.8V_{PP}$ output swing on a single +5V supply with > 50MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 51 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 698Ω resistors). Separate bias networks would be required at each input. The input signal is then ac-coupled into the midpoint voltage bias. The input voltage can swing to within 1.1V of either supply pin, giving a $2V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (59Ω) used for testing is adjusted to give a 50Ω input load when the parallel combination of the biasing divider network is included.


Copyright © 2007–2008, Texas Instruments Incorporated

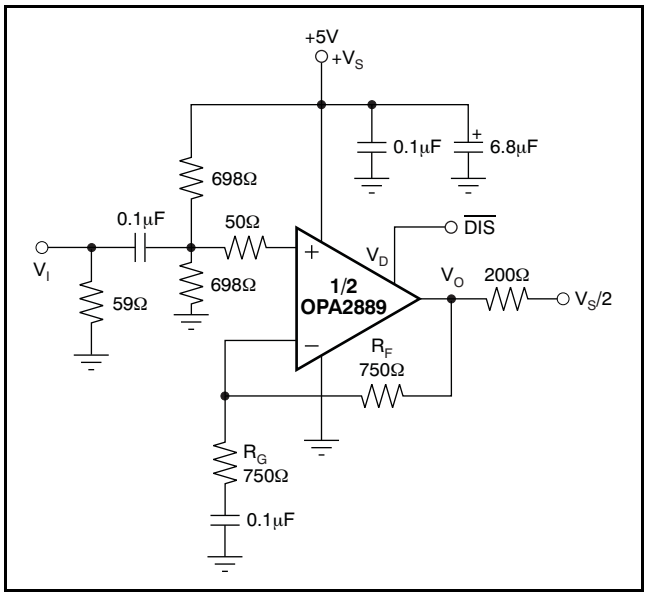



**Figure 51. DC-Coupled, G = +2, Single-Supply, Specification and Test Circuit**

Again, an additional resistor (50Ω in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the dc source resistance matching for the noninverting input bias current. It is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies ( > 500MHz) using the input parasitic capacitance. The gain resistor ($R_G$) is ac-coupled, giving the circuit a dc gain of +1, which puts the input dc bias voltage (2.5V) on the output as well. The output voltage can swing to within 1V of either supply pin while delivering > 40mA output current.

## DIFFERENTIAL OPERATION

Figure 52 shows the inverting input differential configuration used as the basis for the ±5V and +5V Typical Characteristics. This circuit offers a combination of excellent distortion with low quiescent current.

The other possibility is using the OPA2889 in a differential configuration as shown in Figure 53. This figure illustrates the differential noninverting input configuration which has the advantage of showing a high input impedance to any prior stage.

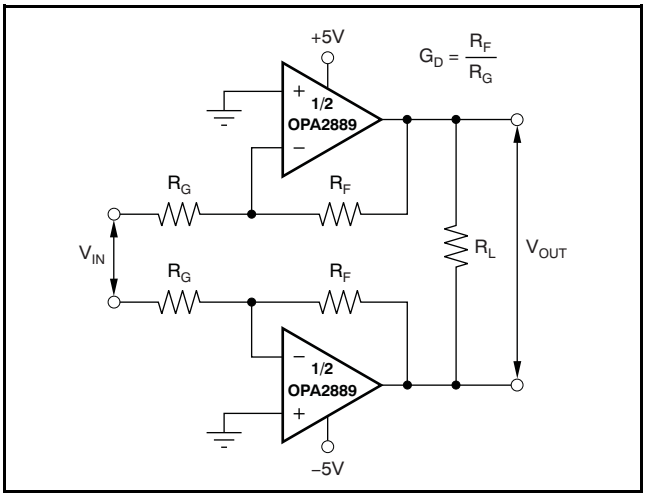



**Figure 52. Differential Inverting Specification and Test Circuit**

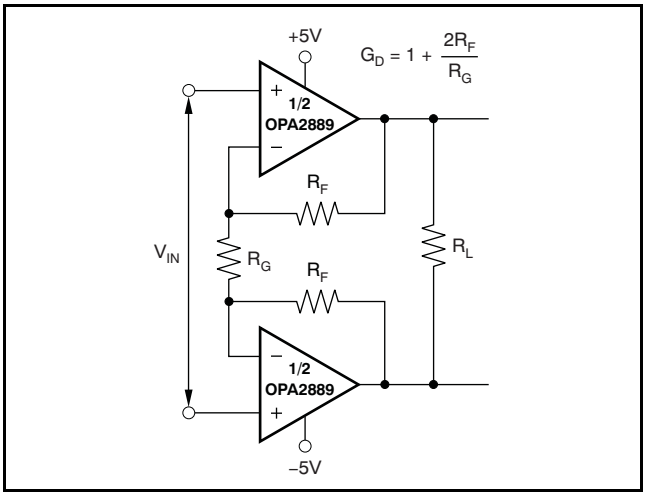



**Figure 53. Differential Noninverting Specification and Test Circuit**

**e) Socketing a high-speed part like the OPA2889 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2889 onto the board.

## INPUT AND ESD PROTECTION

The OPA2889 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 64.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2889), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

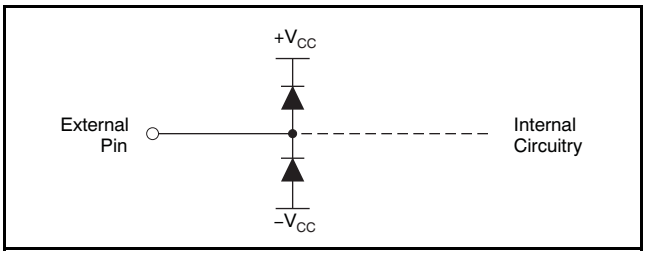



**Figure 64. Internal ESD Protection**


Copyright © 2007–2008, Texas Instruments Incorporated

## Revision History

**Changes from Revision A (September 2007) to Revision B** **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C ..... 2

Copyright © 2007–2008, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| OPA2889ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDGSR | ACTIVE | MSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDGSRG4 | ACTIVE | MSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDGST | ACTIVE | MSOP | DGS | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDGSTG4 | ACTIVE | MSOP | DGS | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA2889IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

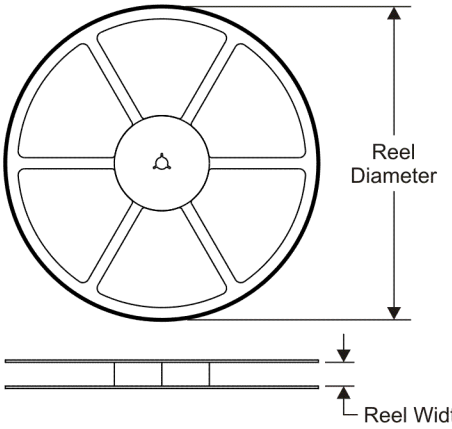
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

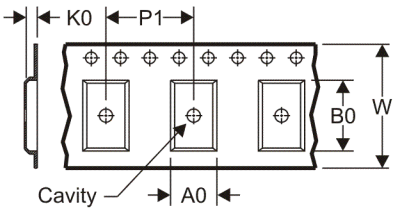
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

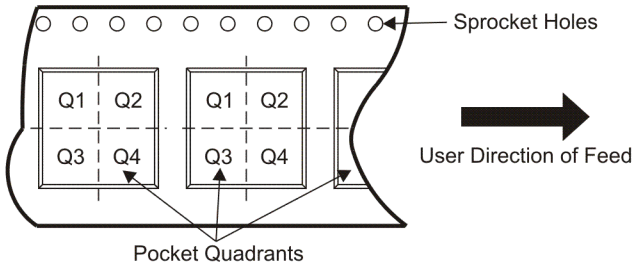



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

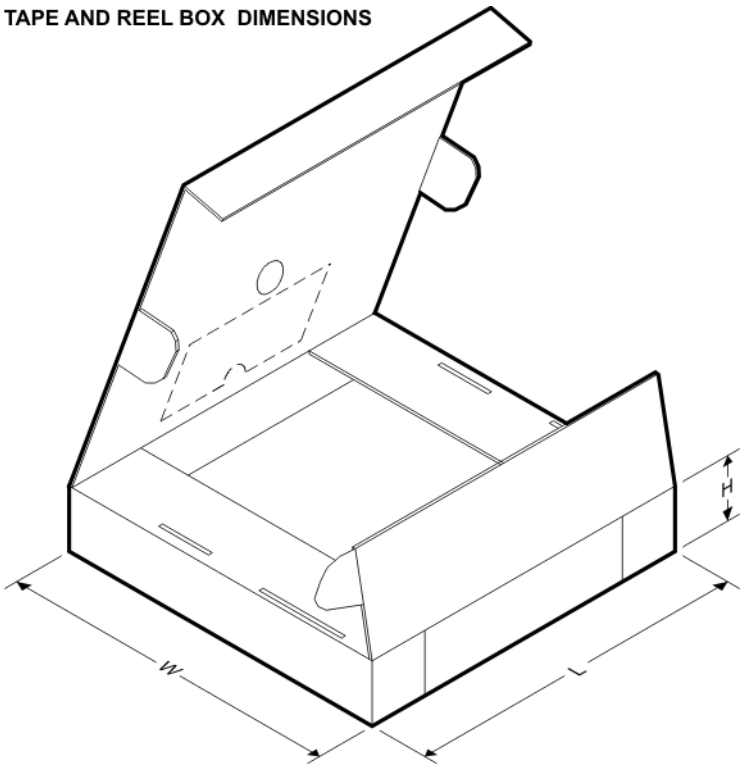
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2889IDGSR | MSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2889IDGST | MSOP | DGS | 10 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2889IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

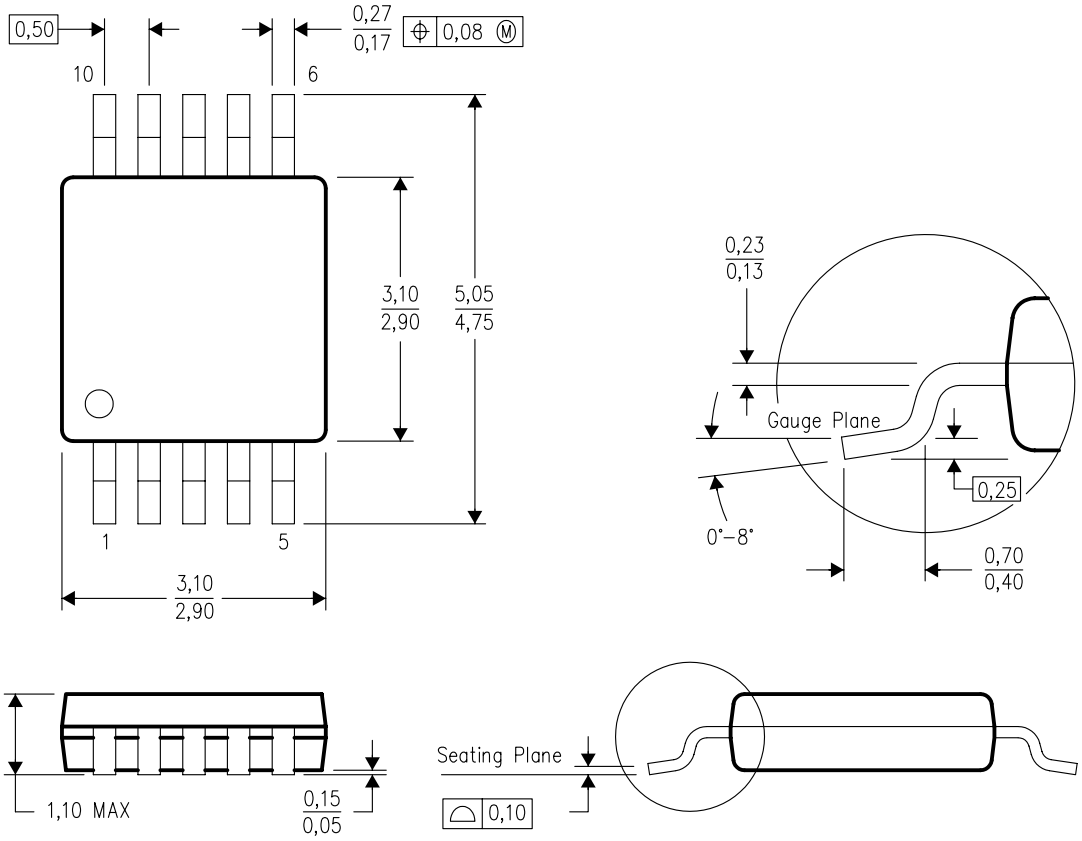
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2889IDGSR | MSOP | DGS | 10 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA2889IDGST | MSOP | DGS | 10 | 250 | 190.5 | 212.7 | 31.8 |
| OPA2889IDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

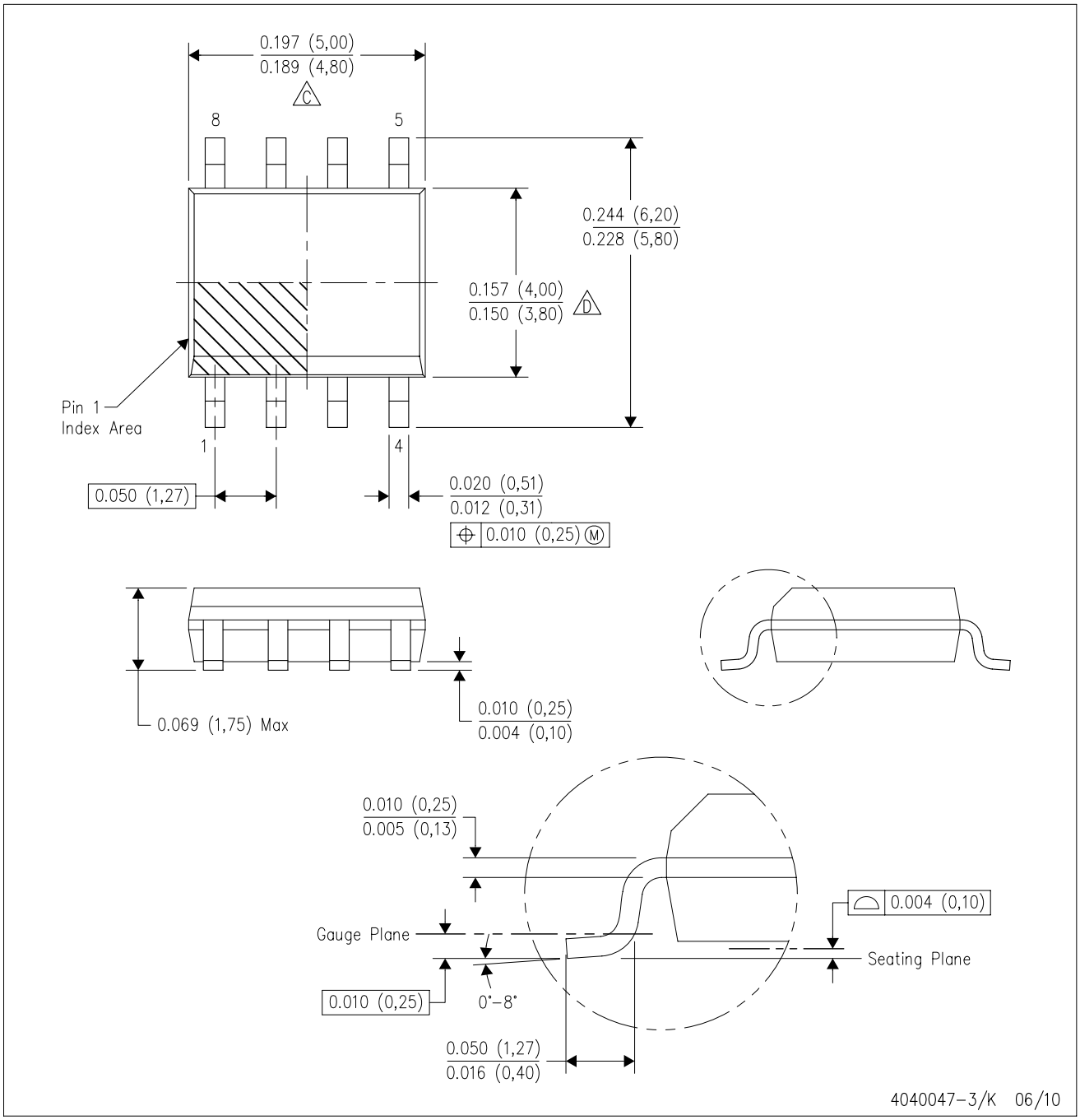
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE




4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DLP® Products | www.dlp.com | Communications and Telecom | www.ti.com/communications |
| DSP | dsp.ti.com | Computers and Peripherals | www.ti.com/computers |
| Clocks and Timers | www.ti.com/clocks | Consumer Electronics | www.ti.com/consumer-apps |
| Interface | interface.ti.com | Energy | www.ti.com/energy |
| Logic | logic.ti.com | Industrial | www.ti.com/industrial |
| Power Mgmt | power.ti.com | Medical | www.ti.com/medical |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Space, Avionics & Defense | www.ti.com/space-avionics-defense |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video and Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless-apps |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated